

**IN THE CLAIMS**

1      1 – 7. (canceled).

1      8. (original) An integrated circuit chip package comprising:  
2            a metal substrate core;  
3            the metal substrate core having at least two electrically isolated regions;  
4            wherein at least one of the electrically isolated regions of the metal substrate core  
5        is coupled with a digital ground of an integrated circuit chip.

1      9. (original) The integrated circuit chip package of claim 8, further comprising:  
2            input and output signals of the integrated circuit chip routed through the  
3            electrically isolated region of the metal substrate core that is coupled with the digital  
4        ground of the integrated circuit chip.

1      10. (original) The integrated circuit chip package of claim 9, wherein at least one  
2        other of the electrically isolated regions of the metal substrate core is coupled with an  
3        operating voltage rail of the integrated circuit chip.

1      11. (original) The integrated circuit chip package of claim 9, wherein at least one  
2        other of the electrically isolated regions of the metal substrate core is coupled with an  
3        analog ground of the integrated circuit chip.

1       12. (original) An integrated circuit chip package comprising:  
2              a metal substrate core;  
3              the metal substrate core having at least three electrically isolated regions;  
4              wherein at least one of the electrically isolated regions of the metal substrate core  
5      is coupled with a digital ground of an integrated circuit chip and has input and output  
6      signals routed through it.

1       13. (original) The integrated circuit chip package of claim 12, wherein at least one  
2      other of the electrically isolated regions of the metal substrate core is coupled with an  
3      operating voltage rail of the integrated circuit chip.

1       14. (original) The integrated circuit chip package of claim 12, wherein at least one  
2      other of the electrically isolated regions of the metal substrate core is coupled with an  
3      analog ground of the integrated circuit chip.

1       15. (original) The integrated circuit chip package of claim 12, wherein at least one  
2      other of the electrically isolated regions of the metal substrate core is coupled with an  
3      operating voltage rail of the integrated circuit chip, and at least one other of the  
4      electrically isolated region of the metal substrate core is coupled with an analog ground  
5      of the integrated circuit chip.

1       16 – 20. (canceled).